⑫ EUROPEAN PATENT APPLICATION

㉝ **Data signal processing apparatus.**

㊗ Apparatus for processing an input data signal includes a generator (64) providing a plurality of pseudo-random signals each of which scrambles the input data signal in one of a plurality of mod. 2-adders (62a to 62d) to provide a plurality of respective scrambled outputs, a detector (65) in which a DC component, such as a run-length or a digital sum value, is detected for each of the scrambled outputs, and a selector (67) responsive to the detector (65) for selecting the one of the scrambled outputs, for example having a minimum run-length or a digital sum value closest to zero. An identifying signal identifying the pseudo-random signal used in scrambling the selected scrambled output is then transmitted with the latter, for example, by recording on a magnetic tape. When the transmitted signal is received or reproduced, the identifying signal included therein is detected, and the received signal is descrambled with a pseudo-random signal corresponding to the detected identifying signal.

FIG. 6

EP 0 343 930 A2

Descripti n

DATA SIGNAL PROCESSING APPARATUS

This invention relates to apparatus for processing input data signals, which apparatus may involve selective scrambling in a channel coding circuit, for example in a digital video tape recorder.

5 A digital video tape recorder (VTR) of a type to which the present invention may be applied will be described with reference to Figure 1 of the accompanying drawings, in which a video signal, for example according to the NTSC system, is supplied to an input terminal 1. The NTSC video signal applied to the input terminal 1 is then supplied to an analog-to-digital (A/D) converting circuit 2 in which it is converted to a digital data signal. The digital data signal is supplied to a bit reduction circuit 3 in which it is reduced in bit number and is then fed to an

10 error correction code (ECC) encoder 4. The ECC encoder 4 adds a parity code for error correction and the like to the data signal. The data signal with parity-code added thereto is supplied to a channel coder 5, in which it is converted to a data series whose characteristic ⌐⌐⌐⌐ ⌐⌐⌐ to the characteristic of a tape head system of the digital VTR. The data series is supplied to an ⌐⌐⌐⌐ circuit 6, in which it is added to a predetermined synchronising (SYNC) code from a synchronising ⌐⌐⌐⌐ generating circuit 7 to provide a recording data signal.

15 The recording data signal which includes the sv⌐ ⌐sing code is supplied from the adding circuit 6 through a recording amplifier 8 to a recording head 9 ⌐ ⌐⌐ thereby recorded on a magnetic tape 10.

Upon playback, a signal reproduced from the magnetic tape 10 by a reproducing head 11 is supplied through a playback amplifier 12 to an equaliser 13, ⌐ which the signal is waveform-shaped in a predetermined manner. The waveform-shaped signal is supplied to a data reproducing circuit 14 which reproduces a data

20 series therefrom. The reproduced data series is supplied to a channel decoder 15 which operates in a manner which is the reverse of the operation of the channel coder 5 provided on the recording side. A synchronising code detecting circuit 28 detects the synchronising code and supplies it to the channel decoder 15. The decoded signal from the channel decoder 15 is supplied to an error correction code (ECC) decoder 16, in which it is error-corrected by the above-mentioned parity code. The error-corrected signal is reduced in bit

25 number by a bit reduction circuit 17 and is then converted from digital to analog form by a digital-to-analog (D/A) converting circuit 18. Finally, the reproduced analog video signal is provided at an output terminal 19.

In the use of the digital VTR of Figure 1 for recording on a previously-recorded tape or other magnetic recording medium, a video signal is generally rewritten by a so-called overwrite system. In such overwriting, if an already recorded signal contains a low frequency component, there is then the risk that a satisfactory erasing characteristic will not be achieved in the next overwrite because the low frequency component is

30 recorded in a relatively deep layer of the tape. Further, there is a substantial possibility that a low frequency component in the signal recorded in adjacent tracks will result in a cross-talk component upon playback.

Furthermore, when a rotary transformer is provided for transmitting signals to and from the head or heads of the digital VTR, the low frequency band that can be transmitted by the rotary transformer is limited so that a

35 low frequency component in the recorded signal causes distortion in the waveform of the reproduced signal.

Therefore, the known digital VTR shown in Figure 1 includes the channel coder 5 and the channel decoder 15 in order to reduce the low frequency component. Figures 2A and 2B of the accompanying drawings illustrate known circuit arrangements that can be used for the channel coder 5 and the channel decoder 15, respectively, and which utilise an M series signal as a pseudo-random signal.

40 In the channel coder 5 shown in Figure 2A, the signal from the ECC encoder 4 (Figure 1) is supplied through an input terminal 21 to a modulo (mod.)2-adder 22 which may be constituted by an exclusive-OR gate. A reset signal associated with a predetermined synchronising block, and which is applied to a reset terminal 23, is supplied therefrom to an M series generator 24. The M series signal from the M series generator 24 is also supplied to the mod. 2-adder 22 which scrambles the M series signal to effect the channel coding. The reset

45 signal applied to the terminal 23 is also supplied to the synchronising code generating circuit 7 which provides the synchronising code. The synchronising code is supplied to the adding circuit 6 in which it is added to the data series from the mod. 2-adder 22, and the resulting added output is applied from an output terminal 25 to the recording amplifier 8 shown in Figure 1.

In the channel decoder 15 shown in Figure 2B, the data signal from the data reproducing circuit 14 (Figure 1)

50 is supplied through an input terminal 26 to a mod. 2-adder 27 which may also be constituted by an exclusive-OR gate. The signal from the input terminal 26 is also supplied to the synchronising code detecting circuit 28 which detects the synchronising code. The detected signal is supplied from the detecting circuit 28 to an M series generator 29 which provides an M series signal to the mod. 2-adder 27 for effecting channel decoding, that is, decoding of the signal scrambled by the M series signal in the channel coder 5. The resulting

55 decoded signal is supplied through an output terminal 30 to the ECC decoder 16 (Figure 1).

The low frequency component in the signal to be recorded is reduced by adding the M series signal to the pseudo-random signal in the mod. 2-adder 22 in Figure 2A, whereby a recording data signal having a reduced low frequency component is generated. Upon playback, the M series signal is added in the mod. 2-adder 27 to the same pseudo-random signal as in the recording mode, resulting in the original data signal being decoded.

60 If the M series signal is added to the pseudo-random signal in a mod. 2-adder to effect the channel coding and the channel decoding as described above, in the absence of any other data signal processing, when a certain relationship is established between the pattern of the recording signal and that of the M series signal, there is the possibility that such a relationship will give rise to the occurrence of a low frequency component.

The occurrence of such a low frequency component is inevitable from a probability standpoint, and this causes deterioration of the overwrite characteristic, the cross-talk characteristic, the waveform characteristic and the like, as described above.

Further, in a digital magnetic recording and reproducing apparatus, such as the above-described digital VTR, if the digital data series (represented in the binary form of "1" or "0") is directly recorded, the following problems arise.

1. The maximum frequency of a recorded signal is increased to such an extent that the recorded signal cannot be read.

2. Direct current and low frequency components frequently appear in the recorded signal so that, when a digital signal is recorded and reproduced by a head system utilising a rotary transformer, distortion occurs in the reproduced signal. As a result, it frequently occurs that the reproduced information deviates considerably from the recorded information.

3. When digital data is recorded, a data series is generally recorded according to the so-called self-clock system together with a clock component. If many digital "1"s or "0"s appear in succession or contiguously, the error rate in extracting the clock component on the playback side is increased.

In order to solve the above-mentioned problem, it is known to arrange a digital magnetic recording and reproducing apparatus so that, upon recording, an input signal is converted to a recording signal having a predetermined frequency characteristic by a channel coding circuit, and this recording signal is recorded on a magnetic recording medium by a recording head. On playback, a signal reproduced from the magnetic recording medium by a playback head is supplied to and is reproduced by a decoder whose converting characteristic is opposite to that of the channel coding circuit. Three channel coding systems are known that are each based on a partial response (PR) system which makes effective use of intersymbol interference in the digital recording. These three channel coding systems will be explained below with reference to Figures 3A to 3D of the accompanying drawings.

A. Non-return to zero-inverted (NRZ-I) system.

In the NRZ-I system, an NRZ signal (Figure 3B), which represents an input signal shown in Figure 3A in the form of a binary code, is converted to an NRZ-I recording signal shown in Figure 3C. The NRZ-I system utilises an encoder to convert the input signal to the recording signal just before the transmission line, and this encoder may be called a precoder. The NRZ-I system precoder is called a PR (1, -1) encoder because it effects the coding, that is conversion, opposite to the conversion of a PR (1, -1) transmission line based on the partial response system. Figure 4A of the accompanying drawings shows an example of a PR (1, -1) encoder which comprises a mod. 2-adder 31 and a one-bit delay circuit 32.

The NRZ-I system has the disadvantage that, when the signal is not inverted, a direct current component frequently appears in the recording signal. Recently, an interleaved NRZ-I (I-NRZ-I) system has been used in order to overcome that disadvantage of the NRZ-I system.

8. Interleaved NRZ-I (I-NRZ-I) system.

According to the I-NRZ-I system, an NRZ signal shown in Figure 3B is converted to an I-NRZ-I recording signal shown in Figure 3D by means of an I-NRZ-I system precoder which performs a conversion reverse to that in a PR (1, 0, -1) transmission line based on the so-called class IV partial response. Such an I-NRZ system precoder is called a PR (1, 0, -1) encoder or a partial response class IV encoder. Figure 4B of the accompanying drawings shows an example of a PR (1, 0, -1) encoder which comprises a mod. 2-adder 31 and two one-bit delay circuits 32a and 32b.

An identifying signal, which results from recording and reproducing the I-NRZ-I recording signal, has frequency characteristics similar to those of the magnetic recording and reproducing system so that it contains fewer high frequency components and does not contain a direct current component. In addition, the identifying signal can be affected by the cross-talk component caused by the increased wavelength of the recording signal and cannot be affected by the rotary transformer.

C. Scrambled I-NRZ-I (S-I-NRZ-I) system.

Although the identifying signal reproduced according to the I-NRZ-I system does not contain a direct current component, the recording signal (see Figure 3D) does contain a direct current component. In order to reduce the direct current component of the recording signal according to the I-NRZ-I system, the S-I-NRZ-I system has been proposed. In accordance with the S-I-NRZ-I system, the M series signal (represented in the form of a binary random number) is added to the input signal in a mod. 2-adder, or the input signal is scrambled by the M series signal, so as to make possible reduction of the direct current component.

Referring now to Figure 5 of the accompanying drawings, it will be seen that, in a previously-proposed digital VTR utilising the S-I-NRZ-I system channel coding circuit, a video signal is applied to an input terminal 43 and is then supplied through a scramble circuit 44 to a PR (1, 0, -1) encoder or precoder 45. The scramble circuit 44 and the PR (1, 0, -1) encoder 45 constitute a channel coding circuit. A recording head 46A with an associated rotary transformer, a magnetic tape 46B and a reproducing head 46C with an associated rotary transformer constitute a PR (1, -1) transmission line 47. A PR (1, 1) decoder 48 is arranged to equalise input data [00100 ...] to provide data [001100 ...]. The PR (1, -1) transmission line 47 and the PR (1, 1) decoder 48 together constitute a PR (1, 0, -1) transmission line 49. A synchronising pulse detecting circuit 50 is operable to detect a

synchronising pulse SYP in the output of a discriminator 48A which is operatively interposed between the PR (1, 1) decoder 48 and the synchronising pulse detecting circuit 50. The digital VTR of Figure 5 further has a descramble circuit 51 and an output terminal 52.

When a recording signal [00100 ...] is supplied from the PR (1, 0, -1) encoder 45 to the recording head 46A, the recording signal is converted, in the PR (1, -1) transmission line 47 (including the recording head 46A, the tape 46B and the reproducing head 46C) to a reproduced signal [001-100 ...]. This reproduced signal [001-100 ...] is supplied to the PR (1, 1) decoder 48 and converted to an identifying signal [0010-100 ...]. The output from the PR (1, 1) decoder 48 is supplied to the discriminator 48A, in which it is processed so that [-1] is changed to [+1]. The resulting identifying signal is identical with the scramble signal [0010100 ...] that is used when the PR (1, 0, -1) encoder 45 generates the recording signal [00100 ...]. Therefore, it is to be understood that a conversion which is the reverse of that effected by the PR (1, 0, -1) encoder 45 is carried out in the PR (1, 0, -1) transmission line 49.

When a certain M series pseudo-random signal Mo is added to the input signal in a mod. 2-adder in the scramble circuit 44, the same pseudo-random signal Mo is added in a mod. 2-adder in the descramble circuit 51 to the identifying signal resulting when the output of the PR (1, 1) decoder 48 is processed in the discriminator 48A such that [-1] is changed to [+1]. In such modulo 2-addition, the addition of the same number results in [000 ...] so that the pseudo-random signal Mo is removed to provide the same data at the output terminal 52 as in the input signal.

Therefore, with the channel coding circuit of the S-I-NRZ-I system, if the input signal has a particular pattern, the direct current component or the low frequency component of the recording signal derived from the PR (1, 0, -1) encoder 45 cannot be reduced by the modulo 2 adding of the pseudo-random signal Mo to the input signal.

According to the present invention there is provided apparatus for processing an input data signal, the apparatus comprising:
generator means for generating a plurality of pseudo-random signals;
scramble means for scrambling the input data signal by each of said plurality of pseudo-random signals and thereby providing a plurality of respective outputs,
detector means for detecting variation of a DC component for each of said outputs of said scramble means;
selector means for selecting one of said outputs of said scramble means under the control of said detector means;
means for adding to said one output selected by said selector means an identifying signal which identifies the pseudo-random signal used in scrambling said one selected output of the scramble means; and
means for transmitting a signal comprising said one output selected by said selector means together with said identifying signal.

A preferred embodiment of the present invention described hereinafter provides an improved selective scramble circuit which can avoid the foregoing problems encountered with the previously-proposed systems.

The preferred selective scramble circuit can carry out the channel coding satisfactorily, can efficiently suppress increasing of data redundancy, can reduce a direct current component in a recording signal regardless of variations in the input signal pattern, and can prevent conversion error from being mixed into a resulting recording signal. The preferred selective scramble circuit is suitable for application to a channel coding circuit of a digital VTR.

The invention will now be described by way of example with reference to the accompanying drawings, throughout which like parts are referred to by like references, and in which:
Figure 1 is a block diagram showing an arrangement of a known digital VTR;
Figure 2A is a schematic block diagram showing an example of a known channel coder used in the digital VTR of Figure 1;
Figure 2B is a schematic block diagram showing an example of a known channel decoder used in the digital VTR of Figure 1;
Figures 3A to 3C are schematic diagrams to which reference is made in explaining channel coding of an input signal;
Figure 4A is a schematic block diagram showing a known partial response class IV (1, -1) encoder;
Figure 4B is a schematic block diagram showing a known partial response class IV (1, 0, -1) encoder;
Figure 5 is a schematic block diagram of a main portion of a previously-proposed digital VTR;
Figure 6 is a block diagram showing an M scramble circuit according to an embodiment of the present invention;
Figure 7 is a diagrammatic view showing a data format to which reference will be made in explaining operation of the present invention;
Figure 8 is a block diagram of a channel decoder according to an embodiment of the present invention;
Figure 9 is a block diagram of a digital VTR according to another embodiment of the present invention;
Figures 10A and 10B form a block diagram showing a selective scramble circuit which may be included in the digital VTR of Figure 9;
Figure 11 is a block diagram of a selective descramble circuit which may be included in the digital VTR shown in Figure 9;
Figure 12 is a diagram showing a data format of the digital data signal used in accordance with an embodiment of the present invention, and which shows the arrangement of one synchronising block;

4

Figure 13 is a diagram showing a data arrangement of an M series identifying code that is used in accordance with an embodiment of the present invention; and

Figures 14A to 14F are timing charts to which reference will be made in explaining the operation of a digital VTR embodying the present invention.

Ref rring to the drawings in d tail, and initially to Figure 6, it will be seen that, in a selective M scramble circuit according to an embodiment of this invention that may be advantageously employed in the digital VTR of Figure 1, an input data signal is supplied through an input terminal 61 to one input of mod. 2-adders 62a, 62b, 62c and 62d. Each of the mod. 2-adders 62a to 62d m constituted by an exclusive-OR gate as shown. A reset signal associated with a predetermined synch block of the input signal is supplied through a reset terminal 63 to an M series generator 64. The M series generator 64 is provided with four output terminals, from which there are derived four M series signals of different phases. The four kinds of M series signals are supplied to respective ones of the adders 62a to 62d.

The output signals from the adders 62a to 62d, that is the input data signal scrambled by the respective M series signals, are supplied to a measuring circuit 65 which measures run lengths and digital sum values (DSV) corresponding to the changes of the direct current components of the respective signals. The circuit 65 is reset in response to the reset signal of each synchronising block and identifies the output signal from the adders 62a to 62d which has the shortest maximum run length and/or the output signal which has the smallest maximum digital sum value in the interval from one synchronising block until the next synchronising block. The run length is determined prior to the digital sum value.

The signals from the adders 62a to 62d are supplied to respective buffer memories 66a to 66d, each of which has a recording or storing capacity of one synchronising block, and are then output therefrom in a first-in first-out (FIFO) fashion. The outputs signals from the buffer memories 66a to 66d are fed to respective fixed contacts 67a to 67d of a switch 67 which is controlled by a switch control signal Sc from the measuring circuit 65.

More particularly, the control signal Sc causes the switch 67 to select the output signal from the one of the buffer memories 66a to 66d, and hence from the respective one of the adders 62a to 62d, which has been determined by the measuring circuit 65 to provide the M scramble signals from the shortest maximum run length and/or the smallest maximum digital sum value. The M scramble signal thus selected is supplied to a data adding circuit 68, in which it is added to a data code identifying or corresponding to the M series signal used for providing the selected M scramble signal.

The signal from the data adding circuit 68 is supplied to a synchronising code adding circuit 69 and the reset signal from the reset terminal 63 is also applied to a synchronising code generating circuit 70 which supplies a synchronising code to the adding circuit 69, whereupon the output signal from the latter is fed to an output terminal 71.

With the above-described selective M scramble circuit, good channel coding is effected by selecting the best one from among a plurality of M scramble signals. Further, by adding data identifying or corresponding to the M series signal used in the coding, it is possible to considerably reduce data redundancy.

The data format of the recording data signal developed at the output terminal 71 is represented in Figure 7, where it will be seen that one synchronising block is formed of a synchronising code SYNC, a data code identifying or corresponding to the M series signal used in the coding and scrambled input data in this order. The data code can be expressed by, for example, two bits such as $a = (0, 0)$, $b = (0, 1)$, $c = (1, 0)$ and $d = (1, 1)$ in the illustrated case where four kinds of M series signals are provided. The increase in data redundancy is very small as a result.

When the circuit shown in Figure 6 is applied to the digital VTR described above with reference to Figure 1, the output signal of the ECC encoder 4 is supplied to the input terminal 61, and the signal from the output terminal 71 is supplied to the recording amplifier 8, whereby recording can be effected in a similar manner to that previously described.

Referring now to Figure 8, it will be seen that, in a decoder according to an embodiment of this invention for use in the playback mode of the digital VTR of Figure 1, a signal applied to an input terminal 82 is supplied to a mod. 2-adder 83 again constituted by an exclusive-OR gate. The signal from the input terminal 82 is also supplied to a synchronising code detecting circuit 84 which detects the synchronising code. The detected signal is supplied from the detecting circuit 84 to an M series generator 85 which can be the same as the M series generator 64 shown in Figure 6. Four kinds of M series signals that differ in phase from each other are supplied from the generator 86 to respective fixed contacts 86a, 86b, 86c and 86d of a switch 86. The signal from the input terminal 82 is also supplied to a data code identifying circuit 87 which identifies the above-mentioned data code corresponding to the kind of M series signal used for the coding. The switch 86 is controlled by this identifying code so as to select from the generator 85 the M series signal which is the same as that used in the recording mode.

The M series signal selectively derived from the switch 86 is supplied to the mod. 2-adder 83, and the signal from the adder 83 is fed to an output terminal 88. In this way, the data signal can be decoded. When the decoder describ d above with reference to Figure 8 is applied to th digital VTR of Figur 1, the output of the data reproducing circuit 14 in Figure 1 is supplied to the input terminal 82, and the signal from the output terminal 88 is supplied to the ECC decoder 16 in Figure 1.

In the circuits of Figures 6 and 8, the M series generators 64 and 85 are not limited to those which provide the M series signal with different phases but they may be M series generators of the type providing M series

signals having different recurrent cycles.

With the circuits of Figure 5 and 8 included in the digital VTR of Figure 1, upon playback, it becomes possible to reproduce a clock signal with ease.

According to the present technique, as set forth above, good channel coding can be effected by selecting
5   the best one from among the plurality of M scramble signals. Further, the increase in data redundancy is suppressed considerably by adding to the input or information signal data identifying the M series signal used in the coding.

Another embodiment of the present invention to which the class IV partial response system can be applied will now be described with reference to Figures 9 to 11 in which parts corresponding to those described with
10   reference to Figure 5 are identified by the same reference numerals and will not be again described in detail. In this embodiment, the technique embodying the present invention is particularly applied to the channel coding circuit of the digital VTR.

It will be seen in Figure 9 that an input terminal 43 receives a digital input signal x(t), in which t is time, and this digital input signal x(t) has been processed to have an error correction code, for example, a cyclic
15   redundancy check code (CRCC) and a parity code.

A selective scramble circuit 93 embodying the present invention receives the digital input signal x(t) and includes a pseudo-random signal adding circuit and a plurality of PR (1, 0, -1) encoders or precoders used in the channel coding. By this selective scramble circuit 93, the digital input signal x(t) is converted to a recording signal y(t) having a reduced high frequency component and a reduced direct current component. The
20   recording signal y(t) is processed by a PR (1, -1) transmission line 47 formed by the recording head 46A with its associated rotary transformer, the magnetic tape 46B and the reproducing head 46C with its associated rotary transformer to provide a reproduced signal. The reproduced signal is fed to the PR (1, 1) decoder 48, and the output signal from the PR (1, 1) decoder 48 is processed by the discriminator 48A so that [-1] is converted to [+1]. The identifying signal Ud(t) derived from the discriminator 48A is supplied to the
25   synchronising pulse detecting circuit 50 which separates the synchronising pulse SYP from the identifying signal Ud(t). A selective descramble circuit 94 is connected to the synchronising pulse detecting circuit 50 and receives therefrom the synchronising pulse SYP and the identifying signal Ud(t). The selective descramble circuit 94 is made to correspond to the selective scramble circuit 93 so as to remove the pseudo-random signal from the identifying signal Ud(t), and to supply the resulting output signal xd(t) to the output terminal 52.
30   The selective scramble circuit 93 will now be described more fully with reference to Figures 10A and 10B, in which a block synchronising pulse BLSY of cycle H is supplied to an input terminal 115 from the external circuit. M series generating circuits 116A, 116B, 116C and 116D are provided to generate respective M series signals M1, M2, M3 and M4 which are different from one another so as to constitute pseudo-random signals. These M series signals M1 to M4 are supplied to mod. 2-adders 117A to 117D, arranged to perform the
35   mod. 2-addition thereto of the input data signal x(t), and which may each be constituted by, for example, an exclusive-OR gate. Three-input multiplexers 118A to 118D receive the outputs of the mod.2-adders 117a to 117d, respectively, and identifying codes from identifying code generating circuits 119A to 119D, respectively, which correspond to the M1 to M4 series signals. The identifying codes generated by the identifying code generating circuits 119A, 119B, 119C and 119D are referred to as code 1, code 2, code 3 and code 4,
40   respectively. Further, a synchronising pulse generating circuit 120 is provided to generate the synchronising pulse SYP which is also supplied to each of the multiplexers 118A to 118D.

The block synchronising pulse BLSY is supplied to the M series generating circuits 116A to 116D so that the latter are initialised at every cycle H. then, signals r1(t) to r4(t) of the M1 to M4 series, respectively, generated by the M series generating circuits 116A to 116D are added in mod. 2 to the input signal x(t) by means of the
45   mod. 2-adders 117A to 117D. The output signals of the mod. 2-adders 117A to 117D, the identifying codes from the identifying code generating circuits 119A to 119D and the synchronising pulse SYP generated by the synchronising pulse generating circuit 120 are supplied to the multiplexers 118A to 118D, respectively, in which they are combined in a time-division manner to generate signals u1(t) to u4(t), respectively.

Each of the time series of multiplexed signals u1(t) to u4(t) is a cyclic signal of cycle H, and the signal format
50   of one synchronising block of cycle H is represented in Figure 12. Such synchronising block is shown to comprise synchronising pulses SYNC0 and SYNC1 each of one byte, data identifying codes (program number, etc) ID0 and ID1 each of one byte and an M series identifying code MSID1 of one byte. The identifying code MSID1 is followed by audio or video data DATA of k bytes, an error correction code, for example, a parity code, of m bytes, and an M series identifying code MSID2 of the same data format as the identifying code MSID1. The
55   area S1 of the block formed of the data identifying codes ID0 and ID1 and the area S2 formed of the data and the error correction code are scrambled by the M series signals.

The M series identifying codes which were referred to above as the codes 1, 2, 3 and 4, and which selectively constitute the M series identifying codes MSID1 and MSID2, are represented as [00000000], [01010101], [10101010] and [11111111], respectively, as shown in Figure 13.
60   With such an arrangement, data of two bits ([00], [01], [10] or [11]) is shown to be repeatedly written four times for each of the codes 1, 2, 3 and 4, respectively, so that even when an error occurs in the transmission system, the identifying code of the M series being used can be positively read. Further, in the embodiment being here described, the M series identifying code MSID2 is of the same format as the code MSID1 and is located distant from each M series identifying code MSID1 by (k + m) bytes. Thus, regardless of the
65   occurrence of burst error, the identifying code can be accurately read on the basis of either one of the M series

identifying codes MSID1 and MSID2.

Referring back to Figures 10A and 10B, it will be seen that the output signals ul(t) to u4(t) from the multiplexers 118A to 118D are respectively supplied to partial response (PR) class IV (1, 0, -1) encoders 121A to 121D acting as precoders, and in which the signals u1(t) to u4(t) are respectively converted to signals y1(t) to y4(t). The PR (1, 0, -1) encoders 121A to 121D are all similarly constructed and, by way of example, the PR (1, 0, -1) encoder 121A will be described in detail.

The PR (1, 0, -1) encoder 121A is shown to comprise an exclusive-OR gate 122 that carries out the mod.2-addition, a two-input switch circuit 123 and two one-bit delay circuits 124 and 125. The signal y1(t) is supplied from the output of the exclusive-OR gate 122 to a first input terminal of the switch circuit 123, and the switch circuit 123 responds to the level of a control signal J1 from a control circuit 129 to selectively supply one of its two input signals through the one-bit delay circuits 124 and 125, in succession, to an input of the exclusive-OR gate 122.

A four-input switch circuit 126 is shown to receive the signals y1(t) to y4(t) at its four input terminals, respectively. The switch circuit 126 responds to a code of a control signal J5 from the control circuit 129 to select one of the signals y1(t) to y4(t) and to supply such selected signal ys0(t) to the other or second input terminal of the switch circuit 123 in each of the PR (1, 0, -1) encoders 121A to 121D. The signals y1(t) to y4(t) from the encoders 121A to 121D are converted to signals y1(t-H) to y4(t-H), respectively, by delay circuits 127A to 127D each having a delay time of one horizontal period (1H), and are then respectively fed to four input terminals of a switch circuit 128. The switch circuit 128 responds to a code of a control signal J6 also derived from the control circuit 129 to select one of the signals y1(t-H) to y4(t-H) as the recording signal y(t). The recording signal y(t) is recorded on the magnetic tape 46B by means of the recording head 46A.

The control circuit 129 is shown in Figure 10 as including a sequence control circuit 130 which responds to the block synchronising pulse BLSY from the terminal 115 to generate the control signals J1 to J4 supplied to the switch circuits 123 of the encoders 121A to 121D, respectively, and also to generate timing signals used to control the operation of additional hereinafter described circuits included in the control circuit 129. A control signal J7 is also generated by the sequence control circuit 130 and is used to simultaneously switch the multiplexers 118A to 118D.

The control circuit 129 is further shown as including digital sum value (DSV) measuring circuits 131A to 131D. A digital sum value (DSV) of digital data series yi(t) from, for example, a time t1 to a time t2, is defined by the following equation:

$$DSV = \sum_{t=t1}^{t2} ai(t) \qquad \qquad \ldots (1)$$

where yi(t) = 1 results in ai(t) = 1, and yi(t) = 0 results in ai(t) = 0, and further assuming that the digital data series yi(t) is generated bit by bit in synchronism with a clock pulse CK whose unit time is T (Figure 14A).

In the present embodiment, when the digital sum value is converged to zero, a direct current component of the digital data series yi(t) becomes zero. The signals y1(t) to y4(t) are supplied to the DSV measuring circuits 131A to 131D, respectively, which measure the digital sum values DSV1 to DSV4, respectively, during a predetermined period corresponding to a block K (Figure 14C). The resultant digital sum values DSV1 to DSV4 are supplied to a determining circuit 132 within the control circuit 129. The determining circuit 132 determines which of the digital sum values DSV1 to DSV4 generated by the measuring circuits 131A to 131D, respectively, is closest to zero, and supplies a corresponding series number s0 identifying the respective one of the M series signals r1(t) to r4(t) to a switch control circuit 133. If the digital sum values of the signals y1(t) to y4(t) are measured for one synchronising block K in which time t ranges from TK (= 0) to TK+1 (= TK + H), in the next time t from TK+1 to TK+2, the one of the signals y1(t) to y4(t) of the block K whose digital sum value is closest to zero is selected by the switch circuit 128 under the control of the switch control circuit 133 to provide the recording signal y(t).

The operation of the embodiment of the invention illustrated in Figures 10A and 10B will now be described with reference to Figures 14A to 14F.

The output signal Us(t) of each of the multiplexers 118A to 118D is expressed, when the respective M series identifying code and the synchronising pulse SYP are removed therefrom, by the following equation:

$$Us(t) = x(t) + rs(t) \pmod 2; = 1 \sim 4 \qquad (2)$$

The output signal ys(t) of each of the PR (1, 0, -1) encoders 121A to 121D is expressed as follows:

$$ys(t) = ys(t-2) + Us(t) \pmod 2 \qquad (3)$$

If it is assumed that data becomes effective from time t = 0, that ys(-2) = ys(-1) = 0 is determined to initialise the PR (1, 0, -1) encoders 121A to 121D, and that the time t is updated at every cycle T (= unit time 1) of the clock pulse CK (Figure 14A) and is expressed as t = 2m or t = 2m + 1, equations (2) and (3) yield:

$$= \sum_{i=0}^{m} x(2i) + \sum_{i=0}^{m} rs(2i) \pmod{2} \qquad \ldots(4)$$

$$ys(t=2m+1) = \sum_{i=0}^{m} x(2i+1) + \sum_{i=1}^{m} rs(2i+1) \pmod{2} \qquad \ldots(5)$$

The DSV measuring circuits 131A to 131D measure the digital sum values during the measuring period K from time t = TK + α to t = TK+1 - 1. In such a case, the following equation (6) is established.

αmin ≦ α ≦ αmax - 2   (6)

In which αmin is determined by the time required to compare the digital sum values and to determine the minimum value, and αmax corresponds to the length of the synchronising pulses SYNC0 and SYNC1. The portions of the synchronising block constituted by the synchronising pulses SYNC0 and SYNC1 are not scrambled so that the digital sum value in the period of TK ≦ t < TK + α is not measured. The digital sum value, which is not measured, is too small to reduce the effects that the present technique achieves.

The DSV measuring circuits 131A to 131D measure the digital sum values DSV1 to DSV4 of the respective series at time t = TK+1. The determining circuit 132 in the control circuit 129 compares the digital sum values DSV1 to DSV4 during the time period of three clock pulses, and supplies to the switch control circuit 133 the series number s0 (1 to 4) of the series signals y1(t) to y4(t) corresponding to the digital sum value which is closest to zero. The switch control circuit 133 responds to the series number s0 to provide the signal J5 which controls the operation of the switch 126 as shown in Figure 14D and to provide the signal J6 which controls the operation of the switch 128 as shown in Figure 14E. The switch circuit 128 selectively passes the signal ys (t - H) (s = s0) of the selected series number s0 only during the period of TK+1 + αmin + 3 ≦ t < TK+2 + αmin + 3. Hence, the following equation is established:

y(t) = ys (t - H)   (7)

and the signal supplied to the recording head 46A as the recording signal y(t) is ys (TK + αmin + 3) to ys (TK+1 + αmin + 2).

This means that the switch circuit 128 selectively provides, during the measuring period K, the signal of the series selected during the preceding measuring period K - 1 at a timing delay by 1H, or by the transmission time of one synchronising block.

The switch circuit 126 is used to cause the PR (1, 0-, -1) encoders 121A to 121D to feed-back their output signals y1(t) to y4(t). The switch circuit 126 supplies the output signal ys0(t), selected as the recording signal during the period of TK + αmin + 3 ≦ t < TK+1 + αmin + 3, to the respective second input terminals of the switch circuits 123 of the PR (1, 0, -1) encoders 121 to 121D during the period of two clock pulses, that is, during the time period TK+1 + αmin 1 ≦ t < TK+1 + α + 3 in which the PR (1, 0, -1) encoders 121A to 121D are initialised. In the time period in which the PR (1, 0, -1) encoders 121A to 121D are initialised, each switch circuit 123 selectively supplies to the delay circuit 124 the signal ys0(t) supplied to the switch circuit 123 from the switch circuit 126, whereby the switch circuit 126 and the switch circuits 123 in the plurality of PR (1, 0, -1) encoders 121A to 121D are operated in association with one another. More specifically, within the precoder initialisation period, TK+1 + αmin + 1 ≦ t < TK+1 + αmin + 3, the output signal ys0(t), which is selected as the recording signal during the period of TK+1 + αmin + 1 ≦ t < TK+1 + αmin + 3, is fed back to the input terminals of the PR (1, 0, -1) encoders 121A to 121D instead of the output signals y1(t) to y4(t).

Generally, the delay circuits 124 and 125 in the PR (1, 0, -1) encoders 121A to 121D delay the output signals by two bits and feed the delayed output signals back to the input terminals thereof. Accordingly, in the absence of the described operation of the switch circuit 126, the output signal y2(t), instead of the recording signal y1(t) in the preceding period, would be fed back to the input terminal of the PR (1, 0, -1) encoder 121B when the recording signal, for example, is switched from the output signal y1(t) of the PR (1, 0 -1) encoder 121A to the output signal y2(t) of the PR (1, 0, -1) encoder 121B, with the result that the succeeding recording signal is made different from the original one. However, the switch circuit 126 is provided to enable the PR (1, 0, -1) encoders to be initialised during a predetermined period of time so that even when the recording signal is switched, accurate signals are invariably fed back to the input terminals of the PR (1, 0, -1) encoders 121A to 121D.

By reason of the switch circuit 126 and the plurality of switch circuits 123, the output signals ys(t) of the PR (1, 0, -1) encoders 121A to 121D can be precisely expressed as:

ys(t) = ys(t-2) + us(t) (mod. 2)   (8)

where t ≠ TK + αmin + 3 and t ≠ TK + αmin + 4, and can also be expressed as

ys(t) = ys0(t-2) + us(t) (mod. 2)   (9)

where t = TK + αmin + 3 and t = TK + αmin + 4, and ys0(t) represents the signal selected as the recording signal in the time period f t < TK + αmin + 3. If it is assumed in equations (8) and (9) that ys (-2) = ys (-1) = 0, then equations (4) and (5) yield

$$ys(t=2m) = \sum_{i=0}^{m} x(2i) + \sum_{i=0}^{m} sx(2i) \ (\text{mod. } 2); \ s = 1 - 4 \quad ...(10)$$

$$ys(t=2m+1) = \sum_{i=0}^{m} x(2i+1) + \sum_{i=0}^{m} rsx(2i+1) \ (\text{mod. } 2) \quad ...(11)$$

In equation (11), $rsx(2i+1)$ represents, if the present time t lies in a range of $TK + \alpha min \leqq t < TK+1 + \alpha min$, a pseudo-random signal $rs0(t)$ ($s0 = 1$ to 4) of the series selected during the period of $(2i+1) \leqq TK + \alpha min$. In the time period of $TK + \alpha min < (2i+1)$, $rsx(2i+1)$ represents pseudo-random signals $r1(t)$ to $r4(t)$ corresponding to the PR (1, 0, -1) encoders 121A to 121D, which fact is expressed by the following equations:

$rsx(t) = rs0(t) : t \leqq TK + \alpha min$ (12)
$rsx(t) = rs(t) : t > TK + \alpha min$ (13)

The PR (1, 0, -1) encoders 121A to 121D generate the output signals that had once contained the pseudo-random signals selected at every synchronising block. The signal y(t), selectively produced from the switch circuit 128 at the time t, is a signal that is delayed by 1H (one horizontal period) after being scrambled by the selected pseudo-random pattern. The signal y(t) is expressed by the following equations

$$y(t) = ys0 \ (t-H)$$
$$= \sum_{i=0}^{m} x(2i-H) + \sum_{i=0}^{m} rs0 \ (2i-H) \ (\text{mod. } 2);$$
$$t = 2m \quad ...(14)$$

$$y(t) = ys0 \ (t-H)$$
$$= \sum_{i=0}^{m} x(2i-H+1) + \sum_{i=0}^{m} rs0 \ (2i-H+1) \ (\text{mod. } 2);$$
$$t = 2m + 1 \quad ...(15)$$

The arrangement of the reproducing side of the digital VTR of Figure 9, and particularly of the descramble circuit 94 included therein, will now be described with reference to Figure 11 in which parts corresponding to those described with reference to Figure 9 are identified by the same reference numerals and are not again described in detail.

In Figure 11, it will be seen that the PR (1, 1) decoder 48 comprises a one-bit delay circuit 134 and an exclusive -OR gate 135 forming a mod. 2-adder. The PR (1, 1) decoder 48, in association with the recording head 46A, the magnetic tape 46B and the playback head 46C, constitutes the PR (1, 0, -1) transmission line 49 which is equivalent to the illustrated circuit comprising two one-bit delay circuits 136 and 137 and an exclusive -OR gate 138, namely, a mod.2-adder. The PR (1, 0, -1) transmission line effects a conversion opposite to the conversion of the channel coding performed by the PR (1, 0, -1) encoders 121A to 121D in the example shown in Figure 10, thereby generating the identifying signal Ud(t). The identifying signal Ud(t) corresponds to the signals U1(t) to U4(t) shown in Figure 10.

The synchronising-signal-recorded-portions SYNC0, SYNC1 and the M series identifying code-recorded-portions MSID1, MSID2 in the identifying signal Ud(t) are not scrambled by the use of a pseudo-random signal, as shown in Figure 12. Hence, the identifying signal Ud(t) is supplied to the synchronising pulse detecting circuit 50, in which the synchronising pulse SYP of a predetermined pattern can be reliably separated from the identifying signal Ud(t). The selective descramble circuit 94 receives the synchronising pulse SYP and the identifying signal Ud(t) derived from the synchronising pulse detecting circuit 50.

In the selective descramble circuit 94, the identifying signal Ud(t) is supplied to a 1H delay circuit 139 and to first and second registers 140 and 141. The M series identifying code MSID1 shown in Figure 12 is supplied to the first register 140, whereas the M series identifying code MSID2 is supplied to the second register 141. These M series identifying codes MSID1 and MSID2 fed to the first and second registers 140 and 141 are fed therefrom to an error correction circuit 142. The error correction circuit 142 judges every byte of the identifying codes MSID1 and MSID2 in a majority-logic-fashion and supplies at least one byte of the judged result to a third register 143 as a correct identifying code ([00] to [11]).

A control circuit 144 is initialised by the synchronising pulse SYP from the detecting circuit 50 and then

drives the first, second and third registers 140, 141 and 143 in a predetermined timed relationship.

M series generating circuits 145A to 145D are arranged in the same way as the M series generating circuits 116A to 116D of Figure 10. The M series generating circuits 145A to 145D are initialised by the synchronising pulse SYP to generate pseudo-random signals of M1 to M4 series, which are fed to respective input terminals
5 of a four-input switch circuit 146. The switch circuit 146 responds to an identifying code from the third register 143 to selectively produce one of the pseudo-random signals of the M1 to M4 series. This selected pseudo-random signal rs0d(t-H) is supplied to one input terminal of a mod. 2-adding circuit 147 (formed by, for example, an exclusive-OR gate). The output signal Ud(t-H) from the 1H delay circuit 139 is supplied to the other input terminal of the adding circuit 147, and the output signal xd(t) from the adding circuit 147 is fed to
10 the output terminal 52.

The embodiment shown in Figure 11 operates as follows.

The third register 143 stores the M series identifying code of the block K corresponding to the time period $TK \leqq t < TK+1$ of the identifying signal Ud(t) during the time period of $TK+1 \leqq t < TK+2$, and supplies the thus stored M series identifying code to the switch circuit 146. The switch circuit 146 supplies the signal
15 rs0d(t-H) corresponding to the M series identifying code to the adding circuit 147 during the time period of $TK+1 \leqq t < TK+2$. In the signals Ud(t), rs0d(t-H) and xd(t), the legend [d] indicates in each case the possibility that the respective variable will contain an error.

In order to examine the influence exerted by the occurrence of error in the PR (1, 0, -1) transmission line 49, let is be assumed that the input signal yd(t) applied to the recording head 46A, that is, the input to the PR (1, 0,
20 -1) transmission line 49, corresponds to that obtained when an error signal e(t) is added to the recording signal y(t) shown in Figure 10. In other words,

yd(t) = y(t) + e(t)   (16)

and, if t = 2m, from equation (10), the identifying signal Ud(t) which is the output signal from the PR (1, 0, -1) transmission line 49 is expressed by the following equation:

$$Ud(t=2m) = Ud(2m) - yd(2m-2) \ (mod. \ 2)$$
$$= (y(2m) + e(2m)) - (y(2m-2) + e(2m-2))$$
$$= \sum_{i=0}^{m} (x(2i) + rs0(2i)) + e(2m)$$
$$= -\sum_{i=0}^{m-1} (x(2i) + rs0(2i)) + e(2m-2)$$
$$= x(2m) + rs0(2m) + e(2m) + 2(2m-2) \qquad \ldots(17)$$

From a mathematical standpoint, the feature that the addition of mod. 2 is equivalent to subtraction is utilised
40 to derive the equation (17). Similarly, from equation (11), if t = 2m+1, the identifying signal Ud(t) is expressed by the following equation:

Ud(t=2m+1) = x(2m+1) + rs0(2m+1) + e(2m+1) + 3(2m+3) (mod. 2)   (18)

Combining equations (17) and (18) yields

Ud(t) = x(t) + rs0(t) + e(t) + e(t-2)   (19)

45 Further, the output signal xd(t) of the adding circuit 147 can be calculated by the following equation:

xd(t) = Ud(t-H) + rs0(t-H) (mod. 2) = x(t-H) + rs0(t-H) + e(t-H) + (t-H-2) + rs0d(t-H)   (20)

Since the equality, rs0d(t-H) = rs0(t-H) is established when the correct M series signal is selected by the switch circuit 146, equation (20) can be modified to read:

xd(t) = x(t-H) + e(t-H) + e(t-H-2)   (21)

50 Thus, the output signal xd(t) from the adding circuit 147 becomes equal to the output signal from the PR (1, 0, -1) transmission line. The fact that the addition of a number to the same number results in zero in the addition of mod. 2 is utilised to derive the equation (21) from equation (20). If e(t-H) = e(t-H-2) = 0 is established in equation (21), this yields:

xd(t) = x(t-H)   (22)

55 Thus it is to be understood that the input to the circuit shown in Figure 10, that is, the signal x(t), delayed by 1H, is equal to the signal xd(t) which is the output from the circuit shown in Figure 11. When the selective descramble circuit 94 is used as described above, the pseudo-random signal of the same series as the scrambled M series signal is add'd in mod. 2 to the identifying signal Ud(t) so that the scrambled M series signal is r moved from the identifying signal Ud(t) thus making it possible to correctly decode the input signal
60 x(t).

Although in the above-described embodiment shown in Figure 10 the control circuit 129 in the selective scramble circuit 93 measures the digital sum values of the respective output signals y1(t) to y4(t) of the PR (1, 0, -1) encoders 121A to 121D, the control circuit 129 may measure, instead of the digital sum values, the maximum run lengths RUN1 to RUN4, that is, the maximum continuous number of high level [1] bits or low
65 level [0] bits, in th respective output signals y1(t) to y4(t) within predetermined time periods, and then

generate, as the recording signal, the output signal ys(t) which has the shortest of these maximum run lengths RUN1 to RUN4.

While the PR (1, 0, -1) encoders 121A to 121D are utilised as the precoders in the above-described embodiment, a similar technique can be applied t a channel coding circuit which, for example, utilises PR (1, -1) encoders as the precoders.

Furthermore, the addition of the M series identifying code and of the synchronising pulse may be effected, for example, between the switch circuit 128 and the recording head 46A, rather than at the multiplexers 119A to 119D between the mod. 2-adders 117A to 117D and the PR (1, 0, -1) encoders 121A to 121D. In that case, although the M series identifying code and the synchronising pulse are not processed by the channel coding process, no problem is presented if a pattern is selected having reduced high frequency and direct current components.

Since, in accordance with the present technique, the precoders are used to reduce both the maximum frequency of the recording signal and the direct current component, and the pseudo-random signal, which scrambles the input signal, is selected so as to provide the best direct current component of the recording signal which is output from the precoders and to provide the best run length, regardless of the change of the pattern of the input signal, it is possible to substantially suppress and thereby minimise the direct current component of the recording signal.

Further, when the signal constituting the recording signal is switched from the output of a first PR (1, 0, -1) encoder to the output of a second PR (1, 0, -1) encoder, the output signal of the first PR (1, 0, -1) encoder, that is the present recording signal, can be fed back to the input terminal of the second PR (1, 0, -1) encoder by means of the switch circuit 126 so that the recording signal can be positively fed back to the input terminals of the respective PR (1, 0, -1) encoders. Hence, mixing of conversion error into the generated recording signal can be prevented.

Claims

1. Apparatus for processing an input data signal, the apparatus comprising:
generator means (64) for generating a plurality of pseudo-random signals;
scramble means (62a to 62d) for scrambling the input data signal by each of said plurality of pseudo-random signals and thereby providing a plurality of respective outputs;
detector means (65) for detecting variation of a DC component for each of said outputs of said scramble means;
selector means (67) for selecting one of said outputs of said scramble means (62a to 62d) under the control of said detector means (65);
means (68) for adding to said one output selected by said selector means (67) an identifying signal which identifies the pseudo-random signal used in scrambling said one selected output of the scramble means (62a to 62d); and
means (46A, 46B) for transmitting a signal comprising said one output selected by said selector means (67) together with said identifying signal.

2. Apparatus according to claim 1, wherein said transmitting means includes means (46A) for recording said one output selected by said selector means (67) with said information signal on a magnetic tape (46B).

3. Apparatus according to claim 1 or claim 2, wherein said detector means includes means for detecting run-lengths of said outputs of said scramble means (62a to 62d).

4. Apparatus according to claim 1 or claim 2, wherein said detector means includes means (131A to 131D) for detecting digital sum values of said outputs of the scramble means (117A to 117D), and said selector means (132) is operative to select the one of said outputs of the scramble means (117A to 117D) having a digital sum value closest to zero.

5. Apparatus according to any one of the preceding claims, comprising:
receiver means (46C) for receiving a signal transmitted by said transmitting means (46A, 46B);
detector means (50) for detecting said identifying signal in the received transmitted signal; and
descramble means (147) for descrambling the received signal in accordance with a pseudo-random signal corresponding to the detected identifying signal.

6. Apparatus according any one of the preceding claims, comprising precoder means (121A to 121D) for encoding each of said outputs of said scramble means (117A to 117D) to have a predetermined frequency characteristic.

7. Apparatus according to claim 6, wherein said precoder means comprises a partial response encoder means (121A to 121D).

8. Apparatus according to claim 6, wherein said precoder means includes a plurality of partial response encoders (121A t 121D) each comprising feedback circuit means (123 to 125) having a delay (124, 125) for encoding a respective output of said scramble means (117A to 117D) in accordance with a partial response method, and switching means (123, 126) for providing, as a feedback to one of said partial response encoders (121A to 121D), an output signal of another of said partial response encoders.
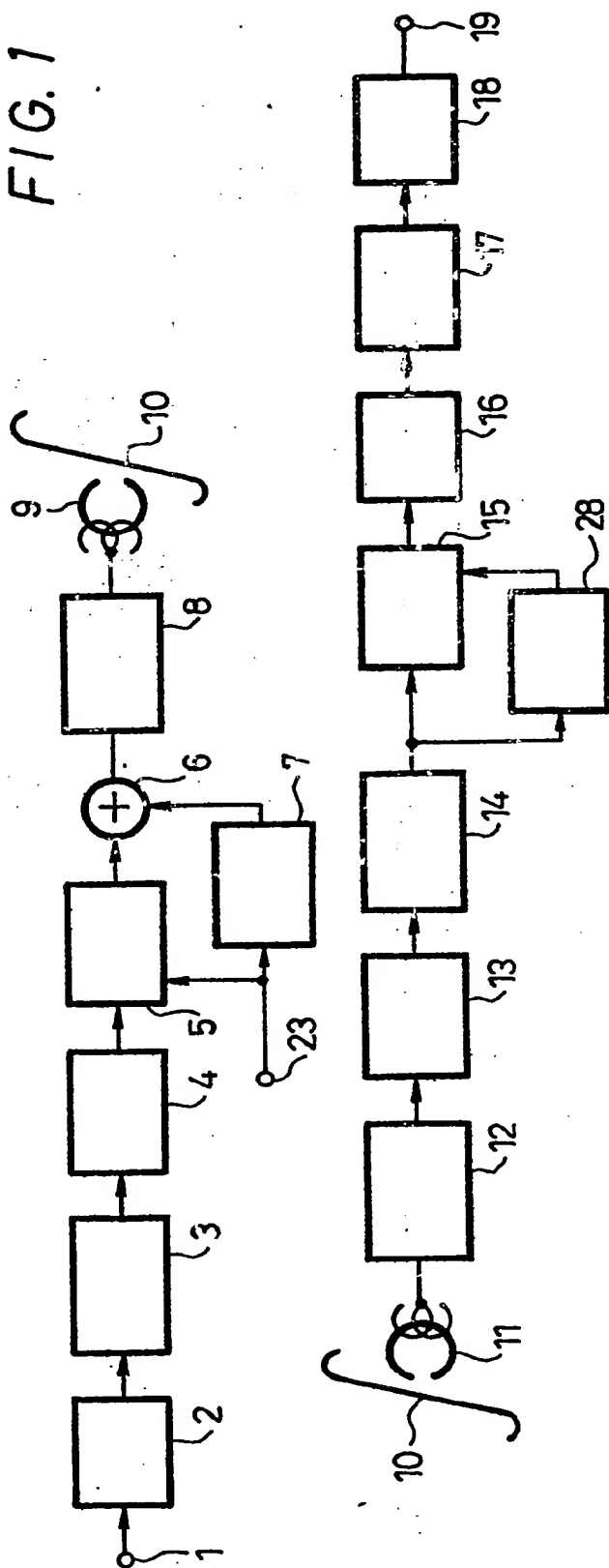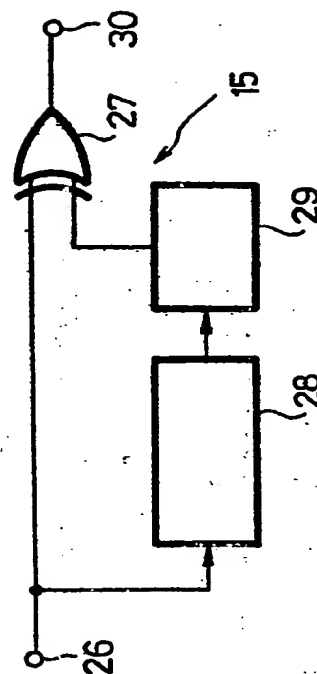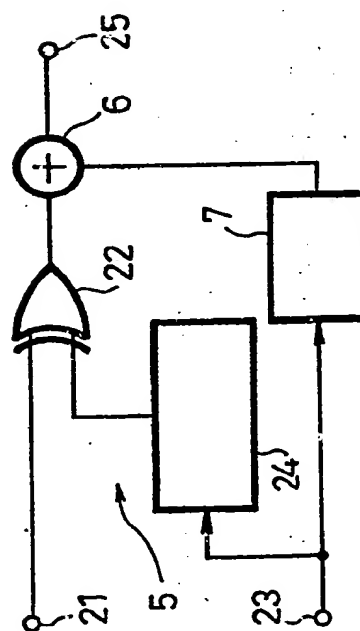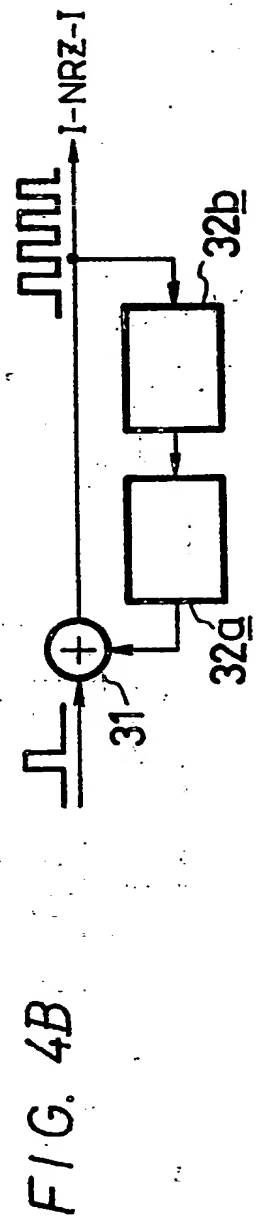
FIG. 1

FIG. 2A

FIG. 2B

FIG. 3A Input Signal |0|0|1|0|0|0|1|1|1|0|0|1|1|1|1|0|0|

FIG. 3B NRZ

FIG. 3C NRZ-I

FIG. 3D I-NRZ-I

FIG. 4A

NRZ-I

31

32

FIG. 4B

I-NRZ-I

31

32a

32b

F I G. 5

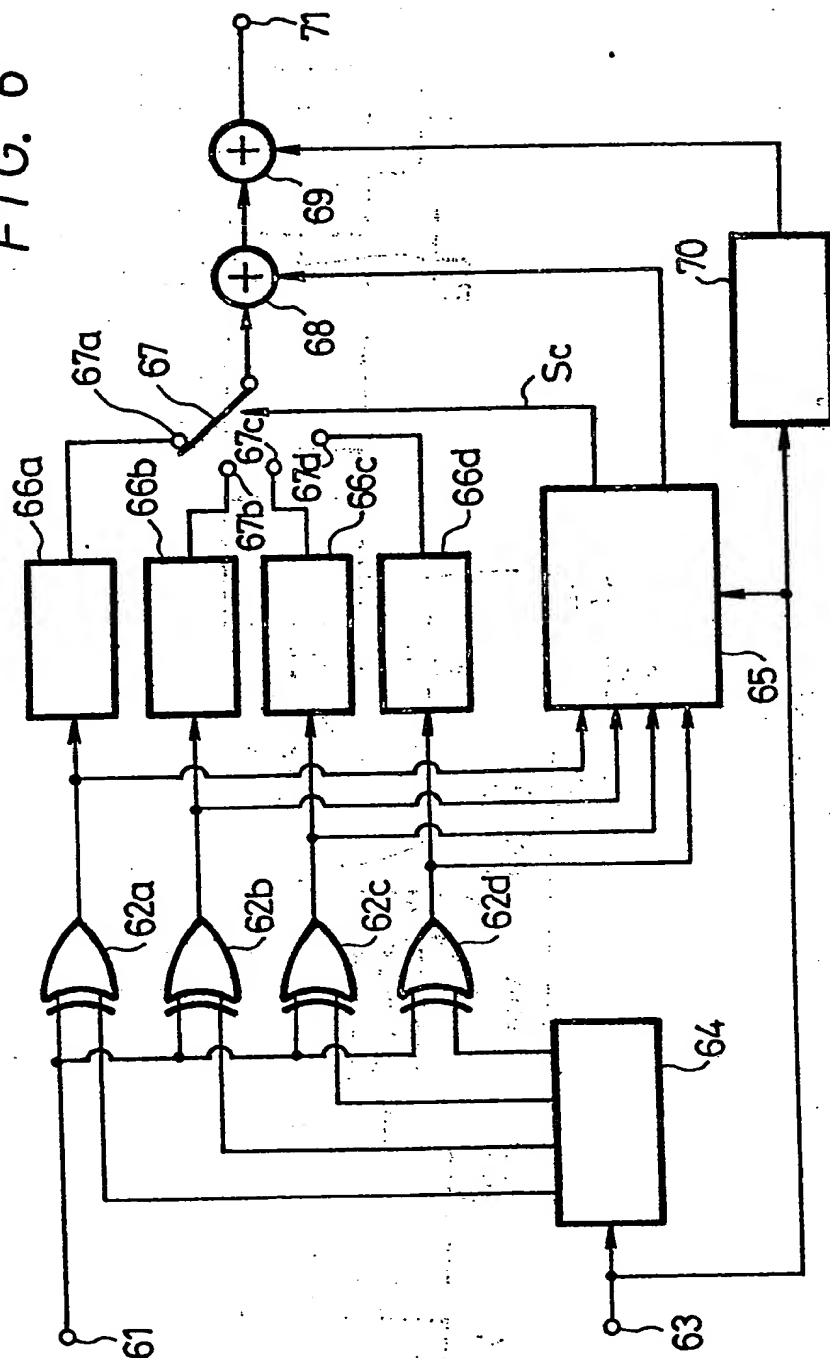# FIG. 6
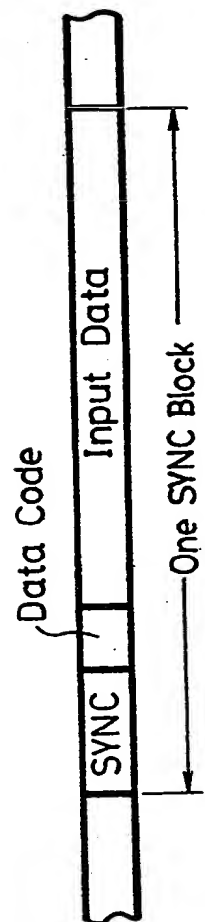
FIG. 7

Data Code

SYNC | Input Data

One SYNC Block
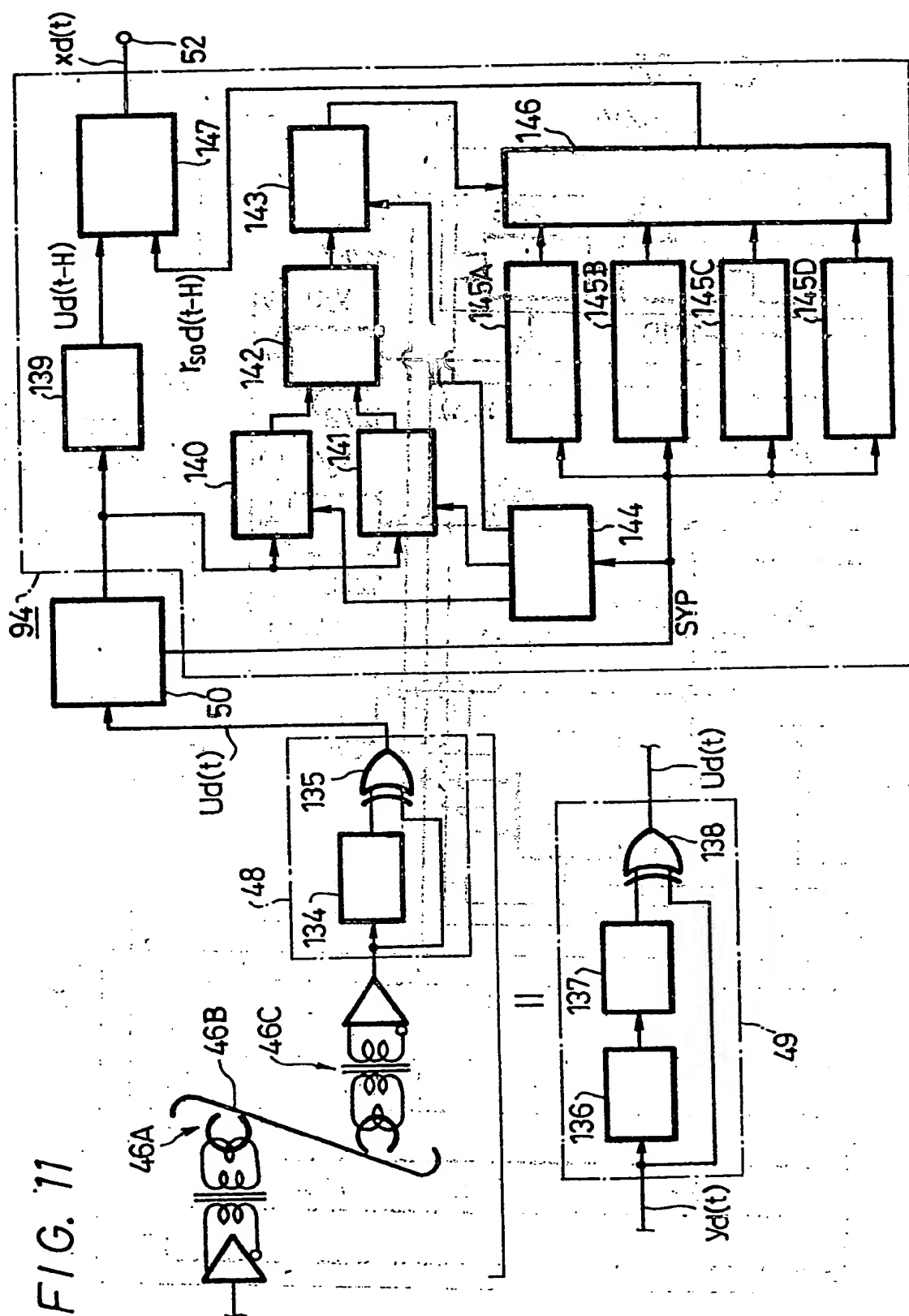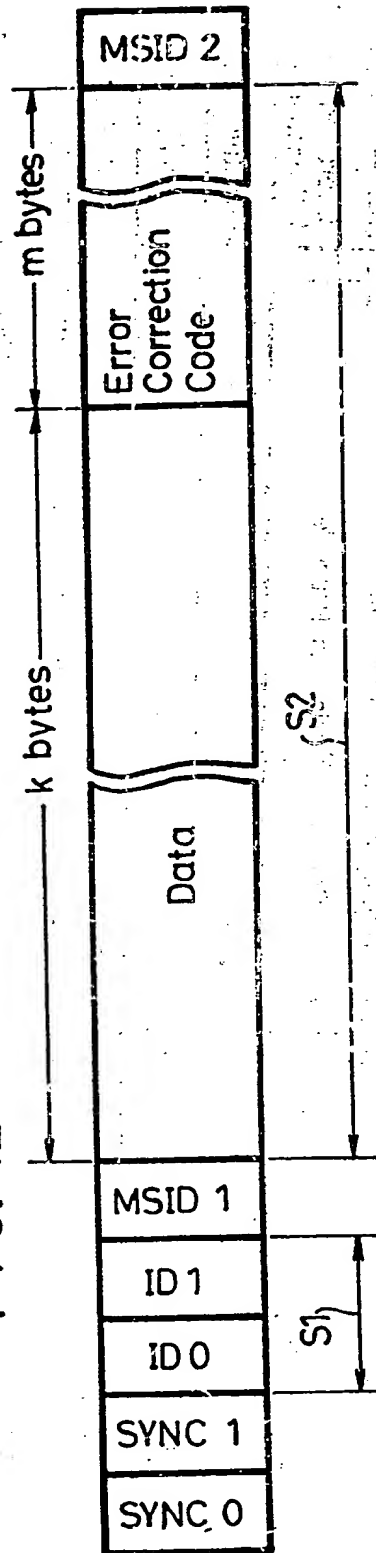
FIG. 8

FIG. 9
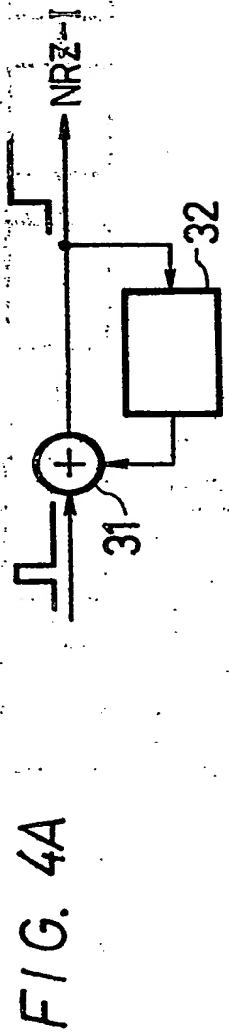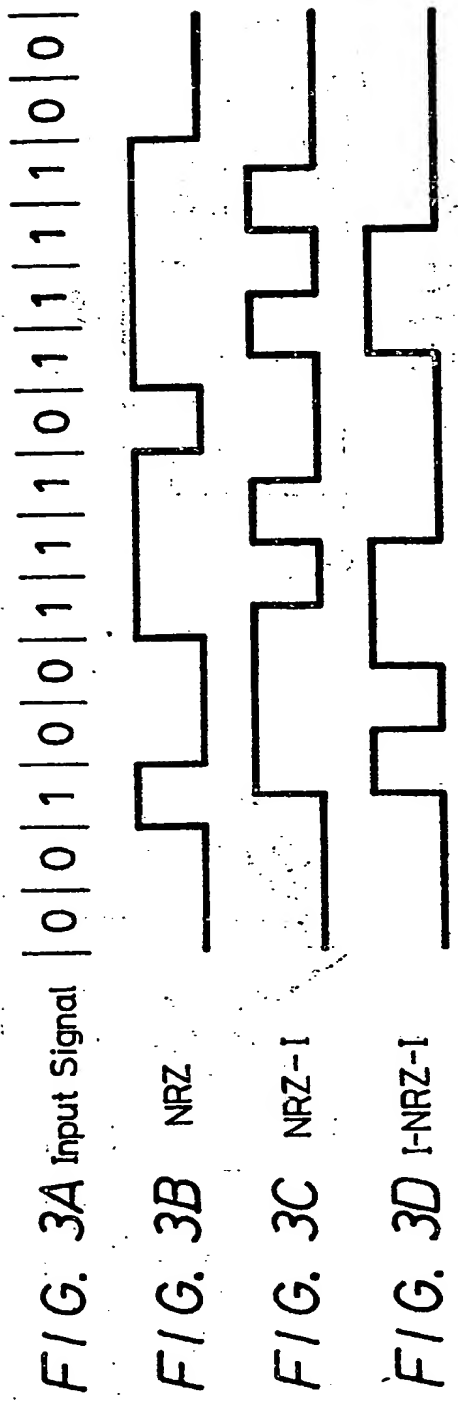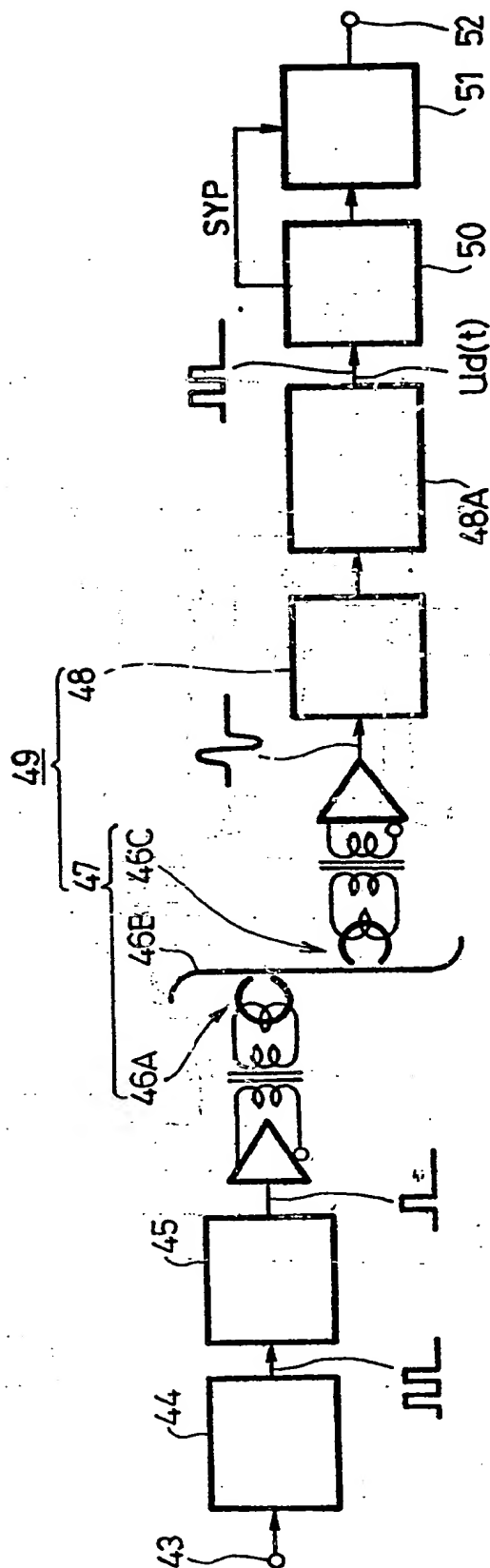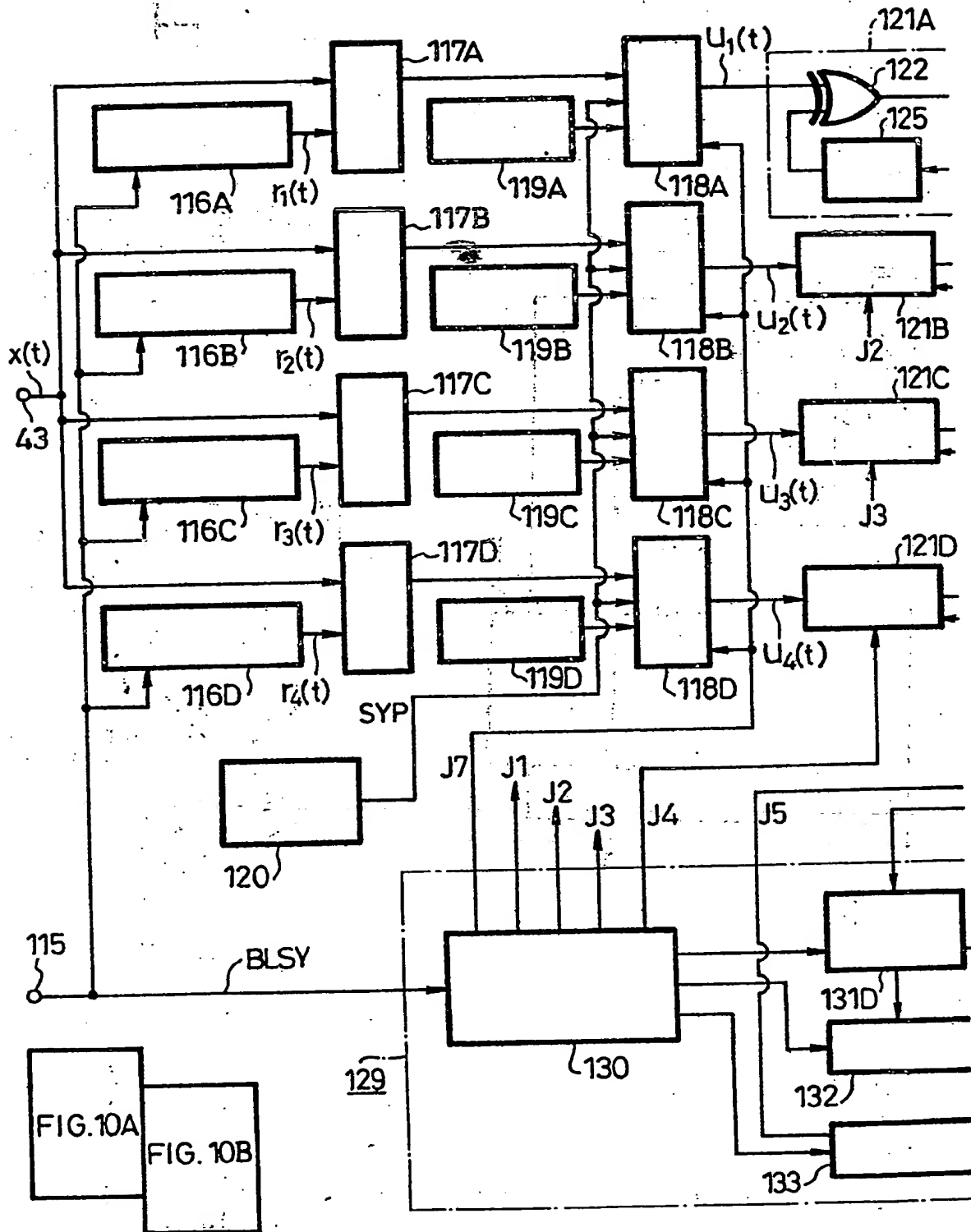
FIG. 10A

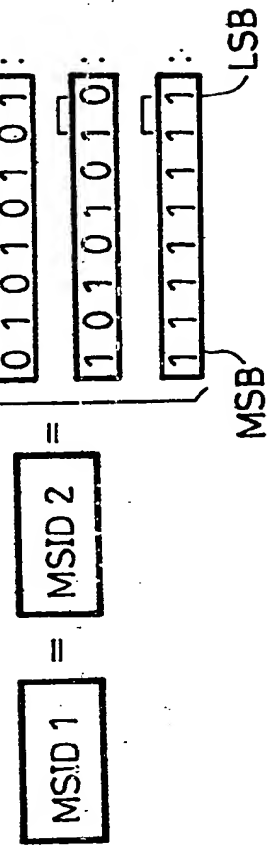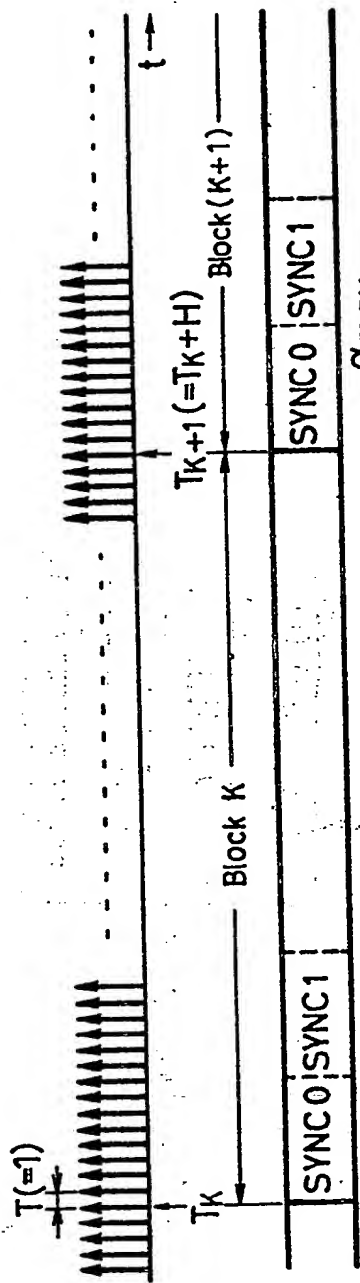# FIG. 10B
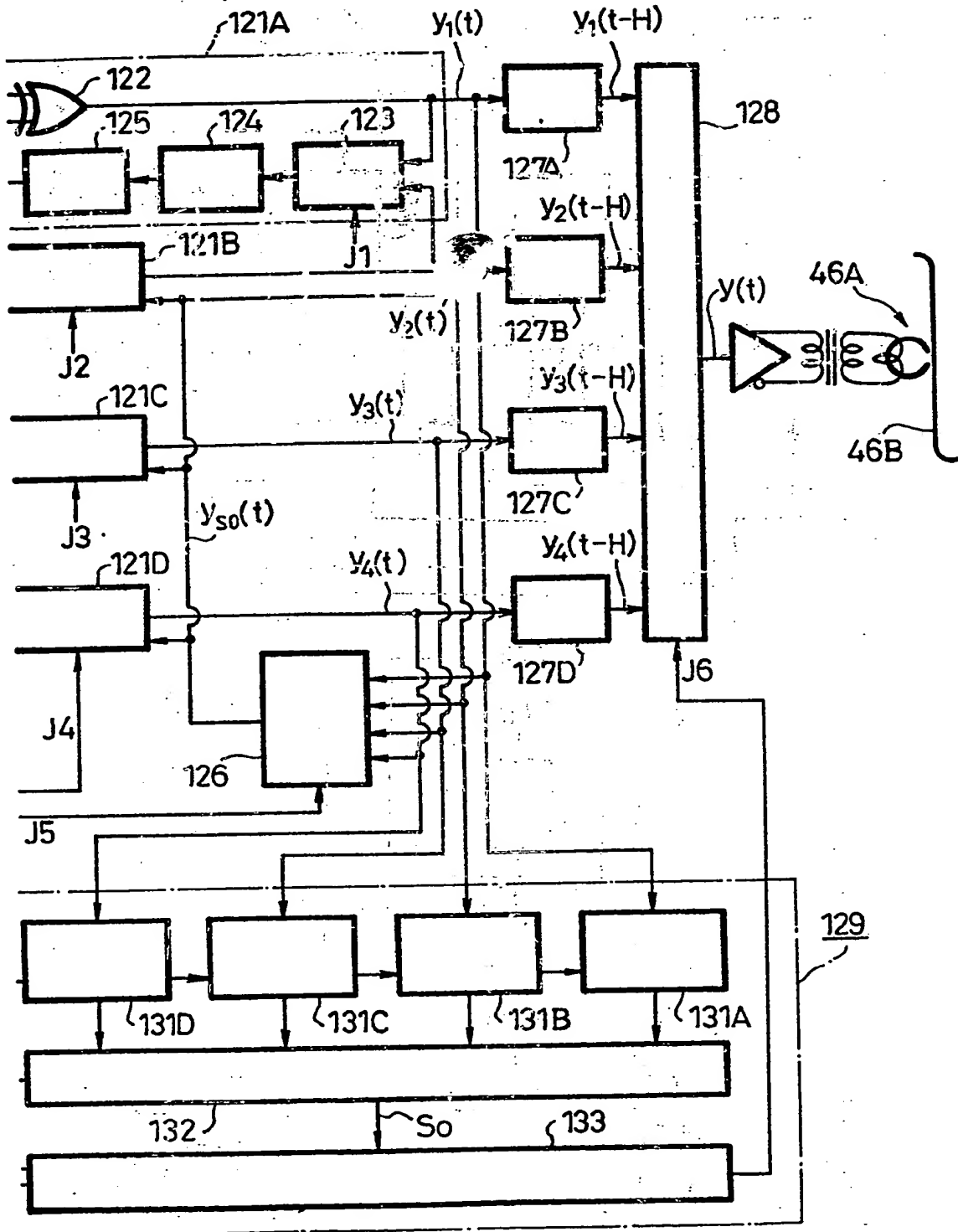
FIG. 11

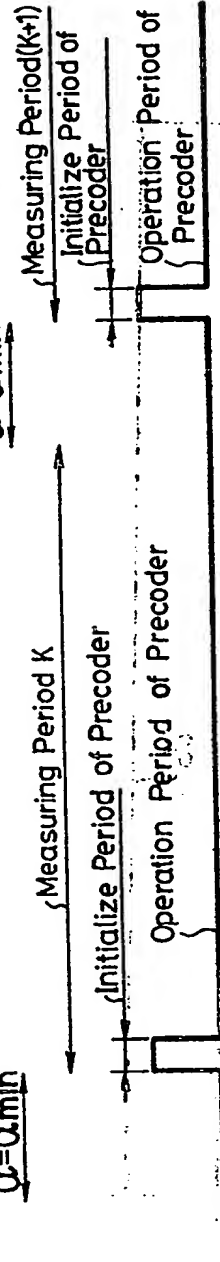FIG. 12

FIG. 13

FIG. 14A Clock Pulse CK

FIG. 14B $y_{s(t)}$

FIG. 14C 123

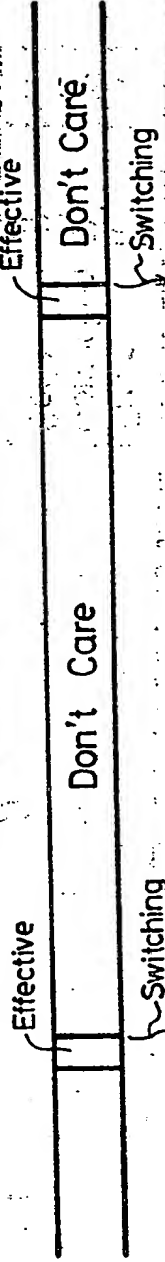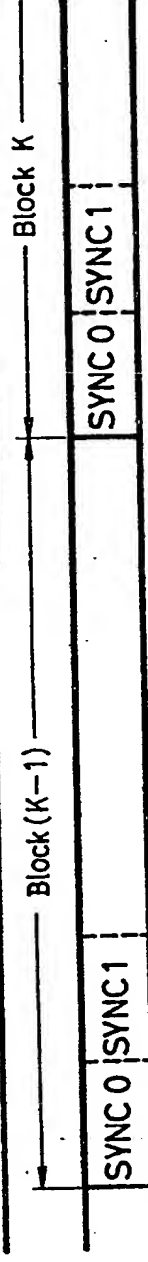FIG. 14D 126

FIG. 14E 128
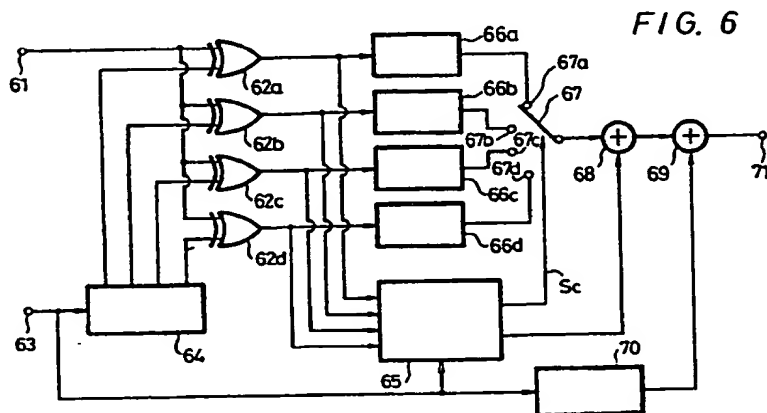
FIG. 14F $y_{s(t-H)}$

⑫ EUROPEAN PATENT APPLICATION

㉒ Inventor: **Kanota, Keiji**
Patents Division Sony Corp. 6-7-35
Kitashinagawa
Shinagawa-ku Tokyo 141(JP)
Inventor: **Nagai, Michio**
Patents Division Sony Corp. 6-7-35
Kitashinagawa
Shinagawa-ku Tokyo 141(JP)

㉔ Representative: **Pilch, Adam John Michael et al**
c/o D. Young & Co. 10 Staple Inn
London WC1V 7RD(GB)

�54 **Data signal processing apparatus.**

�57 Apparatus for processing an input data signal includes a generator (64) providing a plurality of pseudo-random signals each of which scrambles the input data signal in one of a plurality of mod. 2-adders (62a to 62d) to provide a plurality of respective scrambled outputs, a detector (65) in which a DC component, such as a run-length or a digital sum value, is detected for each of the scrambled outputs, and a selector (67) responsive to the detector (65) for selecting the one of the scrambled outputs, for example having a minimum run-length or a digital sum value closest to zero. An identifying signal identifying the pseudo-random signal used in scrambling the selected scrambled output is then transmitted with the latter, for example, by recording on a magnetic tape. When the transmitted signal is received or reproduced, the identifying signal included therein is detected, and the received signal is descrambled with a pseudo-random signal corresponding to the detected identifying signal.

FIG. 6

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
A	EP-A-0 104 700 (N.V. PHILIPS' GLOEILAMPENFABRIEKEN) * page 8, line 28 - page 10, line 28 * ---	1,2,4	G 11 B 20/10 G 11 B 20/14 H 04 N 5/782 H 04 L 25/49
A	US-A-4 301 537 (J. ROOS) * column 3, line 49 - column 5, line 7; figure 1 * ---	1	
A	GB-A-2 149 560 (N.V. PHILIPS' GLOEILAMPENFABRIEKEN) * page 4, line 17 - page 5, line 1; figure 1 * -----	1,4	

TECHNICAL FIELDS SEARCHED (Int. Cl.4)
G 11 B   H 04 L   H 03 M   H 04 J

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	30-05-1990	KELPERIS K.